CLAIMS

I claim:

1. A computer system supported method for preparing a test source file for verifying the performance of a simulated cache memory integrated circuit device design, comprising the steps of:

sequentially and randomly creating a series of functions;

updating a data integrity buffer after each function of said series of functions is created;

creating a series of integrity check functions from said data integrity buffer; and

writing said series of functions and said series of integrity check functions to a test file.

2. The method of claim 1, wherein the data integrity buffer includes a plurality of records, each record of said plurality of records including a cache memory address associated with contents of that cache memory address.

3. The method of claim 2, wherein an address of said each record and contents of said each record are generated at random.

4. The method of claim 3, wherein the data integrity buffer is updated after a normal function is created in said series of functions.

5. The method of claim 4, wherein at least one of the series of functions includes a bitwise memory write operation to a partial word cache memory location and wherein a corresponding integrity check function includes a bitwise memory read operation to read said partial word cache memory location.

6. The method of claim 2, further comprising the steps of reading an entire test settings file into an input buffer before the step of sequentially and randomly creating a series of functions, and further wherein the step of sequentially and randomly creating includes the step of using parameter data from the test settings file to create said series of functions.

7. The method of claim 6, wherein the test settings file includes data directing the generation of prefetch loops.

8. The method of claim 3, wherein the address of each record and the contents of each record are generated at random using the Mitchell-Moore Additive generation method.

9. A digital storage medium having stored thereon a sequence of digital instructions to configure a computer to prepare a test source file for use in verifying the contents of a simulated cache memory integrated circuit device design, the digital instructions defining a sequence of steps for:

sequentially and randomly creating a series of functions;

updating a data integrity buffer in said computer after each function of said series of functions is created;

creating a series of integrity check functions from said data integrity buffer; and

writing said series of functions and said series of integrity check functions to a test file.

10. The method of claim 9, wherein the data integrity buffer includes a plurality of records, each record including a cache memory address associated with contents of that cache memory address.

11. The method of claim 10, wherein an address of each record and contents of each record are generated at random.

12. The method of claim 11, wherein the data integrity buffer is updated after a normal function is created in said series of functions.

13. The method of claim 12, wherein at least one of the series of functions includes a bitwise memory write operation to a partial word cache memory location and wherein a corresponding integrity check function includes a bitwise memory read operation to read said partial word cache memory location.

14. The method of claim 10, further comprising the steps of reading an entire test settings file into an input buffer before the step of sequentially and randomly creating a series of functions, and further wherein the step of sequentially and randomly creating includes the step of using parameter data from the test settings file to create said series of functions.

15. The method of claim 14, wherein the test settings file includes data directing the generation of prefetch loops.

16. The method of claim 11, wherein an address of each record and contents of each record are generated at random using the Mitchell-Moore Additive generation method.

17. A digital computer configured to prepare a test source file for verifying the performance of a simulated cache memory integrated circuit device design, said computer including:

means for sequentially creating a series of functions;

means for updating a data integrity buffer in said computer after each function of said series of functions is created;

means for creating a series of integrity check functions from data in said data integrity buffer; and

means for writing said series of functions and said series of integrity check functions to a test file.

18. The computer of claim 17 further comprising a means for providing test settings to said means for sequentially creating the series of instructions.

19. The computer of claim 18, wherein the data integrity buffer includes a plurality of records, each record including a cache memory address associated with contents of that cache memory address, and further wherein the digital computer further includes a means for randomly generating an address of each record and contents of each record are generated at random.

20. The computer of claim 19, further comprising means for updating the data integrity buffer.

21. The computer of claim 20, wherein the means for updating the data integrity buffer includes means for updating the data integrity buffer after a normal function is created in said series of functions.

22. The computer of claim 21, wherein means for providing test settings to said means for sequentially creating the series of instructions includes means for directing the generation of prefetch loops.